Amendments to the Claims:

1. (withdrawn) An active bias circuit for providing a biasing voltage to an electrical circuit formed on a wafer, the active bias circuit comprising a field effect transistor (FET) having a channel connected to its gate, a biasing current flowing through the FET sets the biasing voltage at the gate of the FET, the FET being formed on the wafer which the electrical circuit is formed to proportionally compensate for variations in the electrical circuit and the active bias circuit as a result of wafer lot to wafer lot variations.

2. (withdrawn) The active bias circuit of Claim 1 wherein an output of the electrical circuit is connected to the channel of the FET.

3. (withdrawn) The active bias circuit of Claim 2 wherein the output of the electrical circuit is a radio frequency signal.

4. (withdrawn) The active bias circuit of Claim1 wherein the FET may be selected from the group consisting of JFET, MOSFET, MESFET, and HEMT.

5. (currently amended) An active bias circuit for providing a biasing voltage to an electrical circuit formed on a wafer, the active bias circuit comprising first and second field effect transistors (FETs), each FET having a channel connected to a gate of the other FET to regulate an amount of current flowing through the channels of the first and second FETs, the current flowing through the second FET sets the biasing voltage at the gate of the first FET, the active bias circuit being formed on the wafer ~~which the electrical circuit is formed~~ to proportionally compensate for variations in the electrical circuit and the active bias circuit as a result of wafer lot to wafer lot variations.

6. (original) The active bias circuit of Claim 5 wherein the first and second FET have a n-type channel.

7. (currently amended) The active bias circuit of Claim 5 wherein an input ~~output~~ of the electrical circuit is connected to the channels of the first and second FETs.

8. (original) The active bias circuit of Claim 7 wherein the output of the electrical circuit is a radio frequency signal.

9. (withdrawn) An amplifier comprising:

a. at least one transistor having an input operative to receive an input signal and amplify the input signal to an output signal which is delivered to an output; and

b. an active bias circuit comprising a field effect transistor (FET) having a channel connected to its gate, a biasing current flowing through the FET sets a biasing voltage at the gate of the FET, the FET is connected to the transistor so as to bias the input signal.

10. (withdrawn) The amplifier of Claim 9 wherein the transistor is formed on a wafer and the active bias circuit is formed on the wafer which the transistor is formed to proportionally compensate for variations in the transistor and the active bias circuit as a result of wafer lot to wafer lot variations.

11. (withdrawn) The amplifier of Claim 9 wherein the output signal provides the biasing current to the FET.

12. (withdrawn) The amplifier of Claim 10 wherein the output signal is a radio frequency signal.

13. (withdrawn) The amplifier of Claim 9 wherein the FET has a N- type channel.

14. (withdrawn) The amplifier of Claim 9 wherein the FETs may be selected from the group consisting of JFET, MOSFET, MESFET, HEMT and pHEMT.

15. (withdrawn) The amplifier of Claim 9 wherein the active bias circuit has high impedance such that the active bias circuit is transparent to the transistor.

16. (withdrawn) An amplifier comprising:

a. at least one transistor having an input operative to receive an input signal and to amplify the input signal to an output signal which is delivered to an output; and

b. an active bias circuit comprising first and second field effect transistors (FETs), each FET having a channel connected to a gate of the other FET to regulate an amount of current flowing through the channels of the first and second FETs, a current flowing through the second FET sets the biasing voltage at the gate of the first FET.

17. (withdrawn) The amplifier of Claim 16 wherein the transistor is formed on a wafer and the active bias circuit is formed on a wafer which the transistor is formed to proportionally compensate for variations in the transistor and the active bias circuit as a result of wafer lot to wafer lot variations.

18. (withdrawn) The amplifier of Claim 16 further comprising a resistive voltage divider connected to the channel of first FET to adjust the biasing voltage at the gate of the first FET.

19. (withdrawn) The amplifier of Claim 16 comprising a sink circuit connected to the gate of the first FET to sink any leakage current from the transistor.

20. (withdrawn) The amplifier of Claim 18 wherein the sink circuit is a resistor and at least one diode connected in series.

21. (new) An electrical circuit comprising:

a. an amplifier circuit formed on a wafer having a designed input biasing voltage for operating the amplifier circuit in an optimal range, the amplifier circuit having a required input biasing voltage offset to operate the amplifier circuit in the optimal range due to wafer lot variations; and

b. an active bias circuit formed on the wafer in electrical communication with the amplifier circuit, the active bias circuit having a designed output biasing voltage and an actual output biasing voltage offset due to the wafer lot variations, the actual output biasing voltage offset being proportional to the required input biasing voltage offset of the amplifier circuit such that the amplifier circuit operates in the optimal range, notwithstanding wafer lot variations.

22. (new) The electrical circuit of Claim 21 wherein the active bias circuit comprises:

i) first and second field effect transistors (FETs), each FET having a channel connected to a gate of the other FET to regulate an amount of current flowing through the channels of the first and second FETs, the source of the second FET connected to the input of the amplifier to bias the amplifier with the biasing voltage;

ii. wherein an actual current draw of the amplifier circuit and FETs of the active bias circuit is greater or less than the designed current draw of the amplifier circuit and FETS due to wafer lot variations, and the increased or decreased current draw through the first FET produces a lower or higher voltage, respectively, at the gate of the second FET to respectively reduce or increase the voltage at the source of the second FET such that the actual output biasing voltage of the active bias circuit has compensated for wafer lot variations.